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(54) SEMICONDUCTOR MEMORY AND ITS CONTROL METHOD

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor memory in which late-write operation by which masking of write data can be performed appropriately is performed and its control method.

SOLUTION: A semiconductor memory has data registers 103-1, 103-2 latching write-in data, DQ write-driver 101-1, 101-2 driving a data line in accordance with write data, DM registers 117-1, 117-2 latching a control signal deciding whether write data is masked or not. In a cycle of a first write command, a first write data is latched in a data register, while a first control signal deciding whether the first write data is masked or not is latched to the DM register conforming to a first data mask signal. In a successive cycle of a second write command, a DQ write-driver is driven conforming to the first control signal latched in the DM register.